

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:

Stephen J. Hudgens

Serial No.: 10/633,873

Filed: August 4, 2003

For: Processing Phase Change Material  
to Improve Programming Speed

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Art Unit: 2826

Examiner: Ahmed N. Sefer

Atty Docket: ITO.0048US  
(P16245)

Assignee: Intel Corporation

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Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**AMENDED APPEAL BRIEF**

Date of Deposit: 01-20-09

I hereby certify that this correspondence is being transmitted electronically to the U.S. Patent Office on the date indicated above.

Janice Munoz  
Janice Munoz

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### **REAL PARTY IN INTEREST**

The real party in interest is the assignee Intel Corporation.

**RELATED APPEALS AND INTERFERENCES**

None.

### **STATUS OF CLAIMS**

Claims 1-10 (Withdrawn).

Claims 11-15 (Canceled).

Claims 16-20 (Rejected).

Claim 21 (Canceled).

Claim 23 (Canceled)

Claims 22 and 24-25 (Rejected).

Claims 26-30 (Withdrawn).

Claims 16-20 and 22-25 are rejected and claim 16 is the subject of this Appeal Brief.

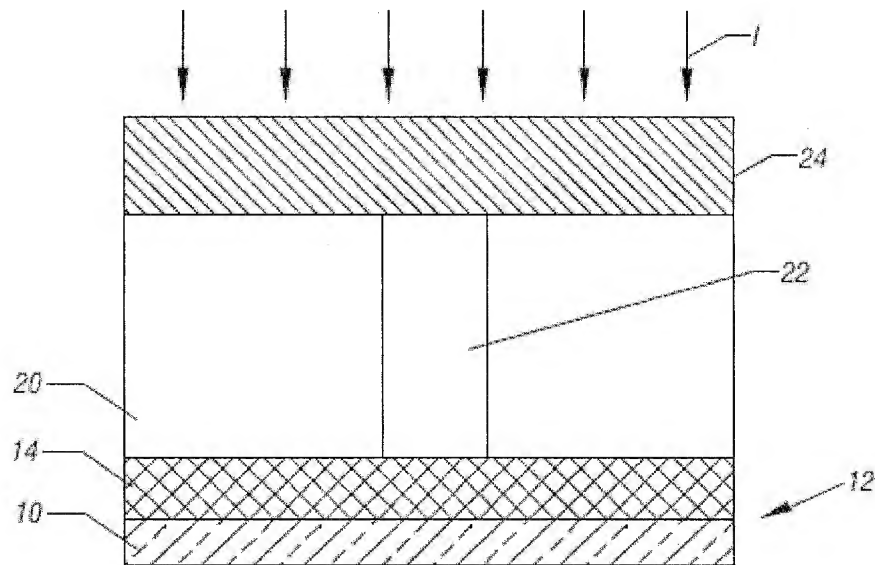
### **STATUS OF AMENDMENTS**

An Amendment is being filed concurrently herewith to incorporate the limitations of claim 23 into independent claim 16.

## SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

16. A semiconductor memory device comprising:  
a semiconductor substrate (Figure 1, 10) (Specification at page 2, lines 18-20);  
and  
a layer of chalcogenide (Figure 1, 24) material over said substrate, said chalcogenide material including a species to reduce the grain size of the chalcogenide material, a species to increase the crystallization speed of said chalcogenide material (Specification at page 3, lines 6-16) and a heater (Figure 1, 22) extending through said insulator to said chalcogenide material to heat said chalcogenide material (Specification at page 2, line 25-page 3, line 3).



**FIG. 1**

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

**GROUND OF REJECTION TO BE REVIEWED ON APPEAL**

- A. Whether claim 16 is unpatentable under 35 U.S.C. § 103(a) over Ichihara in view of Horie (US 2003/0214857).



## ARGUMENT

**A. Whether claim 16 is unpatentable under 35 U.S.C. § 103(a) over Ichihara in view of Horie (US 2003/0214857).**

The rationale for the asserted combination is not clear. The embodiment relied upon in Horie is one in which a conventional semiconductor phase change memory is utilized. But this embodiment in no way suggests any reason to use a layer of chalcogenide material over a semiconductor substrate where the chalcogenide material includes a species to reduce the grain size of the chalcogenide material and a species to increase the crystallization speed. In other words, there is no teaching of any reason to make these changes in a semiconductor phase change memory, as opposed to an optical disk.

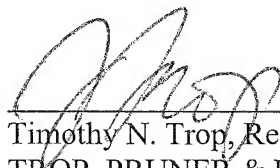
Therefore, rejection of claim 16 should be reversed.

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date:

1/20/09



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Timothy N. Trop, Reg. No. 28,994  
TROP, PRUNER & HU, P.C.  
1616 S. Voss Road, Suite 750  
Houston, TX 77057  
713/468-8880 [Phone]  
713/468-8883 [Fax]

## CLAIMS APPENDIX

The claims on appeal are:

16. A semiconductor memory device comprising:  
a semiconductor substrate;  
a layer of chalcogenide material over said substrate, said chalcogenide material including a species to reduce the grain size of the chalcogenide material and a species to increase the crystallization speed of said chalcogenide material; and  
a heater extending through said insulator to said chalcogenide material to heat said chalcogenide material.
17. The device of claim 16 wherein said chalcogenide material includes  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ .
18. The device of claim 16 wherein the grains of the chalcogenide material are less than approximately 10 nanometers.
19. The device of claim 16 wherein the species to reduce grain size includes nitrogen.
20. The device of claim 16 wherein the species to increase crystallization speed includes titanium.
22. The device of claim 16 including an insulator over said substrate and under said chalcogenide material.
24. The device of claim 16 including titanium containing layer under said chalcogenide material.
25. The device of claim 24 wherein said titanium containing layer is sufficiently proximate to said chalcogenide material that titanium may diffuse into the phase change material upon heating.

## **EVIDENCE APPENDIX**

None.

## **RELATED PROCEEDINGS APPENDIX**

None.